

## **CLAIM AMENDMENTS:**

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the claim number.

Claims 1 - 27 (**canceled**).

1           28. (**NEW**): A semiconductor memory array comprising:  
2           a plurality of memory cells arranged in a matrix of rows and columns, the plurality of  
3           memory cells include a first memory cell and a second memory cell, wherein the first and  
4           second memory cells each include at least a transistor to constitute the memory cell and  
5           wherein the transistor includes:  
6                 a source region;  
7                 a drain region;  
8                 a body region disposed between and adjacent to the source region and the  
9           drain region, wherein the body region is an electrically floating state; and  
10                a gate disposed over the body region;  
11           wherein each memory cell includes:  
12                a first data state representative of a first charge in the body region; and  
13                a second data state representative of a second charge in the body region  
14           wherein the second charge is substantially provided by removing charge from the  
15           body region through the source region; and  
16           wherein the gate of the first memory cell and the gate of the second memory cell are  
17           connected.

1           29. **(NEW)**: The memory array of claim 28 wherein:  
2           the plurality of memory cells further includes a third memory cell and a fourth  
3 memory cell, wherein the third and fourth memory cells each include at least a transistor to  
4 constitute the memory cell and wherein the transistor includes:  
5           a source region;  
6           a drain region;  
7           a body region disposed between and adjacent to the source region and the  
8 drain region, wherein the body region is an electrically floating state; and  
9           a gate disposed over the body region;  
10          wherein each memory cell includes:  
11           a first data state representative of a first charge in the body region; and  
12           a second data state representative of a second charge in the body region  
13 wherein the second charge is substantially provided by removing charge from the  
14 body region through the source region; and  
15          wherein the source region of the first memory cell and the source region of the third  
16 memory cell are the same region wherein the drain region of the first memory cell and the  
17 drain region of the fourth memory cell are the same region.

1           30. **(NEW)**: The memory array of claim 28 wherein the first charge is comprised of  
2 an accumulation of majority carriers in the body region.

1           31. **(NEW)**: The memory array of claim 30 wherein the majority carriers accumulate  
2 in a portion of the body regions that is adjacent to the source regions.

1           32. **(NEW)**: The memory array of claim 28 further including a control unit, coupled  
2 to the gate and the drain region of the first memory cell, to provide control signals to the  
3 first and second memory cells, wherein the first memory cell, in response to a first write  
4 control signal set, stores the first charge in the body region.

1           33. **(NEW)**: The memory array of claim 32 further including a control unit, coupled  
2 to the gate and the drain region of the first memory cell, to provide control signals to the  
3 first and second memory cells, wherein the first memory cell, in response to a second write  
4 control signal set, stores the second charge in the body region by removing charge from  
5 the body region of the first memory cell through its source region.

1           34. **(NEW)**: The memory array of claim 33 wherein the control unit applies positive  
2 voltages to the drain region and gate of the first memory cell to provide the second charge  
3 in the body region.

1           35. **(NEW)**: The memory array of claim 34 wherein the control unit applies positive  
2 voltages to the drain region and gate of the first memory cell to provide the second charge  
3 in the body region and applies a first voltage to the drain and source regions of the second  
4 memory cell to maintain the data state of the second memory cell.

1           36. **(NEW)**: The memory array of claim 35 wherein the first voltage is ground.

1           37. **(NEW)**: A semiconductor memory array comprising:

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a plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cell include a first memory cell and a second memory cell, wherein the first and second memory cells each include at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type,

a body region disposed between and adjacent to the source region and the drain region wherein the body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate disposed over the body region;

wherein the memory cell includes:

a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the gate of the first memory cell and the gate of the second memory cell are connected.

38. **(NEW)**: The memory array of claim 37 wherein:

the plurality of memory cells further includes a third memory cell wherein the third memory cell includes at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide a first conductivity type;  
a drain region having impurities to provide the first conductivity type,  
a body region disposed between and adjacent to the source region and the  
drain region wherein the body region is electrically floating and includes impurities to  
provide a second conductivity type wherein the second conductivity type is different  
than the first conductivity type;  
a gate disposed over the body region; and  
wherein the memory cell includes:  
a first data state representative of a first charge in the body region wherein  
the first charge is substantially provided by impact ionization; and  
a second data state representative of a second charge in the body region  
wherein the second charge is substantially provided by removing charge from the  
body region through the source region; and  
wherein the source region of the first memory cell and the source region of the third  
memory cell are the same region.

39. (NEW): The memory array of claim 37 wherein:  
the plurality of memory cells further includes a fourth memory cell wherein the fourth  
memory cell includes at least a transistor to constitute the memory cell wherein the  
transistor includes:  
a source region having impurities to provide a first conductivity type;  
a drain region having impurities to provide the first conductivity type,  
a body region disposed between and adjacent to the source region and the  
drain region wherein the body region is electrically floating and includes impurities to

9 provide a second conductivity type wherein the second conductivity type is different  
10 than the first conductivity type;  
11 a gate disposed over the body region,  
12 wherein the memory cell includes:  
13 a first data state representative of a first charge in the body region wherein  
14 the first charge is substantially provided by impact ionization; and  
15 a second data state representative of a second charge in the body region  
16 wherein the second charge is substantially provided by removing charge from the  
17 body region through the source region; and  
18 wherein the drain region of the first memory cell and the drain region of the fourth  
19 memory cell are the same region.

1 40. **(NEW)**: The memory array of claim 39 wherein the first charge is comprised of  
2 an accumulation of majority carriers in the body region.

1 41. **(NEW)**: The memory array of claim 40 wherein the majority carriers accumulate  
2 in a portion of the body regions that is adjacent to the source regions.

1 42. **(NEW)**: The memory array of claim 39 further including a control unit, coupled  
2 to the gate and the drain region of the first memory cell, to provide control signals to the  
3 first and second memory cells, wherein the first memory cell, in response to a first write  
4 control signal set, stores the first charge in the body region.

1           43. **(NEW)**: The memory array of claim 42 further including a control unit, coupled  
2 to the gate and the drain region of the first memory cell, to provide control signals to the  
3 first and second memory cells, wherein the first memory cell, in response to a second write  
4 control signal set, stores the second charge in the body region by removing charge from  
5 the body region of the first memory cell through its source region.

1           44. **(NEW)**: The memory array of claim 43 wherein the control unit applies positive  
2 voltages to the drain region and gate of the first memory cell to provide the second charge  
3 in the body region.

1           45. **(NEW)**: The memory array of claim 44 wherein the control unit applies positive  
2 voltages to the drain region and gate of the first memory cell to provide the second charge  
3 in the body region and applies a first voltage to the drain and source regions of the second  
4 memory cell to maintain the data state of the second memory cell.

1           46. **(NEW)**: The memory array of claim 45 wherein the first voltage is ground.

1           47. **(NEW)**: A semiconductor memory array comprising:           <sup>15</sup>  
2 a plurality of memory cells, arranged in a matrix of rows and columns, including a  
3 first memory cell and a second memory cell, wherein the first and second memory cells  
4 each include at least a transistor to constitute the memory cell and wherein the transistor  
5 includes:  
6 a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type,  
a body region disposed between and adjacent to the source region and the  
drain region wherein the body region is electrically floating and includes impurities to  
provide a second conductivity type wherein the second conductivity type is different  
than the first conductivity type;  
a gate spaced apart from, and capacitively coupled to, the body region;  
wherein the memory cell includes:  
a first data state representative of a first charge in the body; and  
a second data state representative of a second charge in the body region  
wherein the second charge is substantially provided by removing charge from the  
body region through the source region; and  
wherein the gate of the first memory cell and the gate of the second memory cell are  
connected.

48. (NEW): The memory array of claim 47 wherein:  
the plurality of memory cells further includes a third memory cell wherein the third  
memory cell includes at least a transistor to constitute the memory cell wherein the  
transistor includes:  
a source region having impurities to provide a first conductivity type;  
a drain region having impurities to provide the first conductivity type;  
a body region disposed between and adjacent to the source region and the  
drain region wherein the body region is electrically floating and includes impurities to  
provide a second conductivity type wherein the second conductivity type is different  
than the first conductivity type;



11 a gate spaced apart from, and capacitively coupled to, the body region;and  
12 wherein the memory cell includes:  
13 a first data state representative of a first charge in the body; and  
14 a second data state representative of a second charge in the body  
15 region wherein the second charge is substantially provided by removing  
16 charge from the body region through the source region; and  
17 wherein the source region of the first memory cell and the source region of the third  
18 memory cell are the same region.

1 49. (NEW): The memory array of claim 48 wherein:  
2 the plurality of memory cells further includes a fourth memory cell wherein the fourth  
3 memory cell includes at least a transistor to constitute the memory cell wherein the  
4 transistor includes:  
5 a source region having impurities to provide a first conductivity type;  
6 a drain region having impurities to provide the first conductivity type;  
7 a body region disposed between and adjacent to the source region and the  
8 drain region wherein the body region is electrically floating and includes impurities to  
9 provide a second conductivity type wherein the second conductivity type is different  
10 than the first conductivity type;  
11 a gate spaced apart from, and capacitively coupled to, the body region; and  
12 wherein the memory cell includes:  
13 a first data state representative of a first charge in the body; and

14 a second data state representative of a second charge in the body region  
15 wherein the second charge is substantially provided by removing charge from the  
16 body region through the source region; and  
17 wherein the drain region of the first memory cell and the drain region of the fourth  
18 memory cell are the same region.

1 50. **(NEW)**: The memory array of claim 47 wherein the second write control signal  
2 set includes a first signal, having a first positive voltage, applied to the drain region of the  
3 first memory cell.

1 51. **(NEW)**: The memory array of claim 50 wherein the second charge is stored in  
2 the body region in response to removing the first positive voltage from the drain region of  
3 the first memory cell before removing the second positive voltage from the gate of the first  
4 memory cell.

1 52. **(NEW)**: The memory array of claim 51 wherein, in response to the first and  
2 second positive voltages, the first memory cell includes a forward bias current between its  
3 body region and its source region.

1 53. **(NEW)**: The memory array of claim 52 wherein the second charge is stored in  
2 the body region of the first memory cell in response to removing the first positive voltage  
3 from the drain region of the first memory cell and wherein the source regions of the first and  
4 second memory cells are connected to a fixed voltage.

1           54. **(NEW)**: The memory array of claim 47 wherein the first charge is comprised of  
2 an accumulation of majority carriers in the body region.

1           55. **(NEW)**: The memory array of claim 54 wherein the majority carriers accumulate  
2 in a portion of the body regions that is adjacent to the source regions.

1           56. **(NEW)**: The memory array of claim 47 further including a control unit, coupled  
2 to the gate and the drain region of the first memory cell, to provide control signals to the  
3 first and second memory cells, wherein the first memory cell, in response to a first write  
4 control signal set, stores the first charge in the body region.

1           57. **(NEW)**: The memory array of claim 56 further including a control unit, coupled  
2 to the gate and the drain region of the first memory cell, to provide control signals to the  
3 first and second memory cells, wherein the first memory cell, in response to a second write  
4 control signal set, stores the second charge in the body region by removing charge from  
5 the body region of the first memory cell through its source region.

1           58. **(NEW)**: The memory array of claim 57 wherein the control unit applies positive  
2 voltages to the drain region and gate of the first memory cell to provide the second charge  
3 in the body region.

1           59. **(NEW)**: The memory array of claim 58 wherein the control unit applies positive  
2 voltages to the drain region and gate of the first memory cell to provide the second charge

3 in the body region and applies a first voltage to the drain and source regions of the second  
4 memory cell to maintain the data state of the second memory cell.

1 60. **(NEW)**: The memory array of claim 59 wherein the first voltage is ground.